Low Power and High-Speed Dynamic D Flip Flop based on Gates Tied GNRFET in 16nm Technology Length

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Abstract— D flip flops are classified into two types: static and dynamic. The dynamic D flip flop is the subject of this study. The complex design of TSPC is accompanied by clock and reset setup (True single phase clocked). When it comes to its job and switching operation, the clock and rest signal absorb a lot of power. This makes it an interesting research field where improvements to the power consumption of the TSPC-based D flip flop are needed. Power consumption increases below 16nm due to effects such as DIBL or GIBL, which must also be improved. In this paper, a new TSPC-based D Flip Flop with Gates Tied Mode (Multi-Threshold CMOS Logic) sleep signal injection is proposed for low power applications to reduce power consumption. To reduce the short channel effects in MOS, this work employs low power dependent MOS such as GNRFET. This paper focuses on low power consumption by the use of GNRFETs in 16nm technology.

Index Terms— DFF, gates tied, GNRFET, TSPC

1 Introduction

D flip-flops are widely used because they are known to be the most fundamental memory cell in the vast majority of digital circuits, especially in current conditions where high-density pipeline innovation is frequently used in digital integrated circuits and massive flip-flop modules are invaluable segments. As a continuous testing centre, numerous types of zero flip-flops have been invented and researched, and the ongoing exploration pattern has shifted to rapid low-control execution, which can be boiled down to a low power-delay product. To realise superior VLSI, selecting the best D flip-flop has simply become an essential part of the design process. The explanations stem from two perspectives: the first is that D flip-flop has a direct effect on the clock recurrence of digital circuit frameworks, especially for certain small-scale structures with shallow sensible depth; the second is that D flip-flop is an essential component of clock organise, accounting for 30% - half of the chip's force dissipation. According to previous research, several standard D flip-flops with outstanding execution have been presented. As is customary, the D Flip-Flop (DFF) proposed in has significantly reduced the simple way delay and cleverly eliminated the beat generator assembly, resulting in the use of a semi-static circuit and a distinct advantage in terms of both speed and force dissipation. DFF has been reinvestigated and updated as a foundational framework of our practise. From another angle, as progress has shrunk, spillage power dissipation has become an increasingly important component of overall force dissipation, and a few standard new devices have been proposed to address this problem. Until now, the most promising new product has been the GNRFET, and market chips have already been launched by major foundries. Currently, is used to replace planar MOSFETs in order to increase the appearance of DFF. In the meantime, taking into account the benefits of various GNRFET working modes, DFF is adjusted to achieve lower power dissipation without sacrificing too much working pace. Right now, improved TSPC D flip-flops with low force delay products based on GNRFETs have been presented. Reduces the force delay product due to improved electrical properties and the unique advantages of multiple operating modes of GNRFET. In the meanwhile, the latter reduces the number of transistors, making it more suitable for high-end digital ICs, as the MOSFET mass has high short-circuit impacts in 32nm and beneath. This determines the proposition's problem articulation.

The use of GNRFETs in the construction of superior dynamic TSPC D flip-flops has been adopted. Based on the amazing electrical properties of GNRFET, the TSPC D flip-flop, which has been changed from special by substituting MOS like GNRFET for planar MOSFET, has a significant reduction in power-delay product (PDP). Given the novel advantages of various GNRFET working modes, more streamlining based on Modified TSPC based on MOSFET like GNRFET has been suggested to achieve lower PDP and increasingly active zone consumption volume. The simulation results show that the Modified TSPC D Flip Flop decreases the PDP while increasing the number of transistors slightly.

2 Implementation

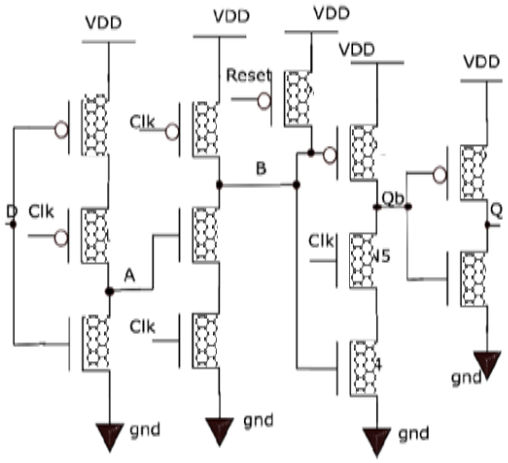

Fig. 1: TSPC based D Flip Flop GNRFET 16nm Proposed

In Fig. 1, the TSPC based DFF is implemented using GNRFET in HSPICE through node coding method. Similarly, 2 Fig. are for GNRFET modified and Gates Tied Mode proposed circuit.

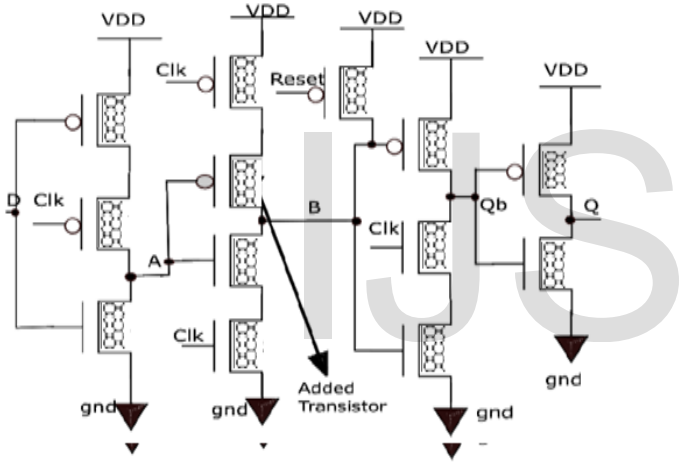

Fig. 2: Modified TSPC based D Flip Flop GNRFET 16nm Proposed

Waveform of TSPCD Flip Flop after GNRFET implementation is shown in Fig. 3 below.

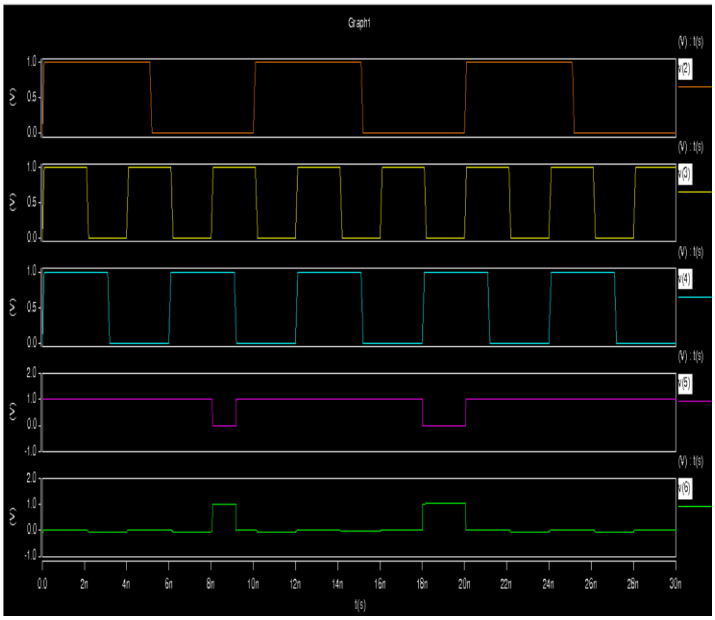

Fig. 3: Output and Input waveforms for GNRFET based TSPC Circuit

Waveform for GNRFET based 16nm modified proposed circuit are shown in Fig. 4.

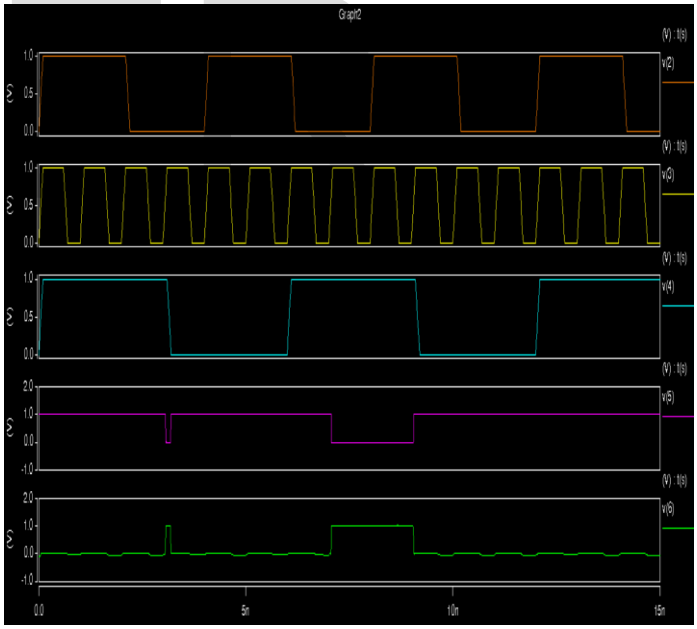

Fig. 4: Output and Input waveforms for Modified GNRFET based TSPC Circuit

3 RESULTS

In this section, results are shown for the performance metrics. The tool used is HSPICE and Cosmoscope for waveform analysis and excel for plotting the results below:

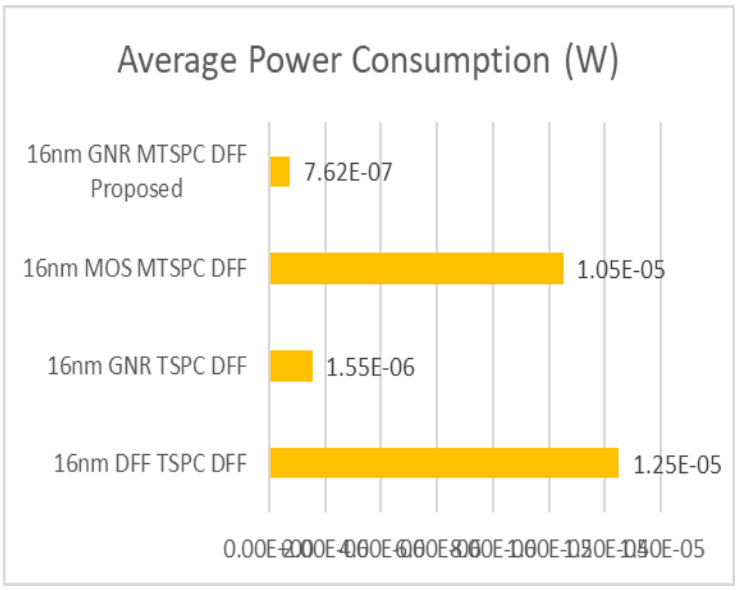

Fig. 5: Average Power Consumption Output for 16nm DFF in all modes

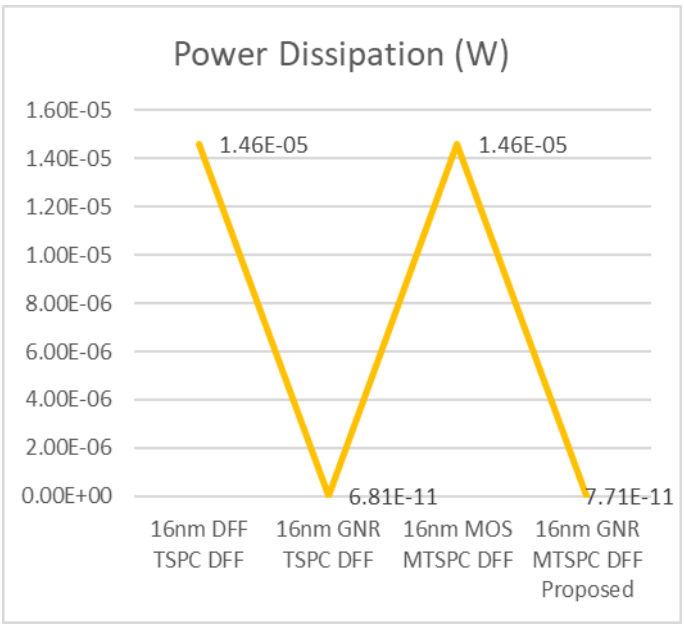

Fig. 7: Power Dissipation Output for 16nm DFF in all modes

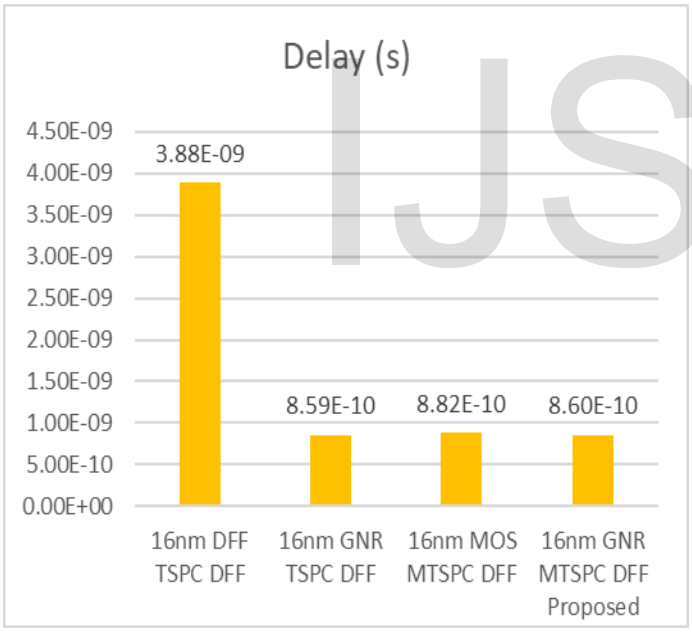

Fig. 6: Delay Output for 16nm DFF in all modes

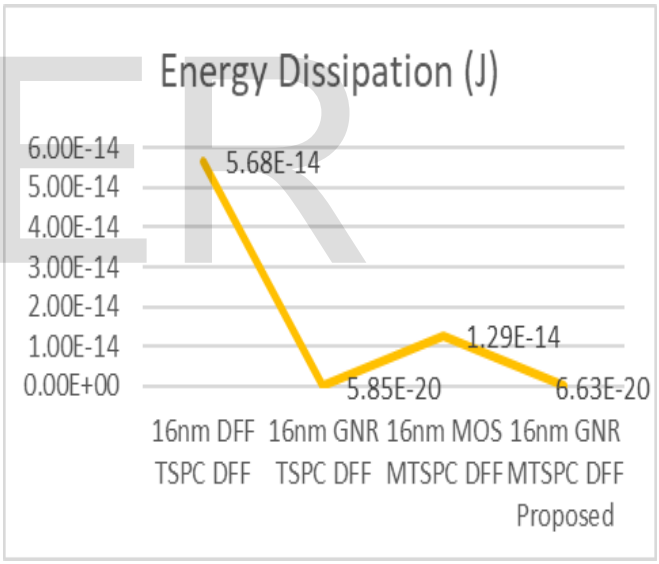

Fig. 8: Energy Dissipation Output for 16nm DFF in all modes

The results are shown in Fig. 5 to 8 for Average power, delay, power dissipation and energy dissipation. In all best performance is for the proposed circuit with GNRFET in 16nm gates tied. In table 1 the result comparison is shown.

Table 1: Comparison Results with Existing Work

	16nm DFF TSPC DFF	16nm GNR TSPC DFF	16nm MOS MTSPC DFF	16nm GNR MTSPC DFF Proposed

Average Power Consumption (W)	1.25E-05	1.55E-06	1.05E-05	7.62E-07
Delay (s)	3.88E-09	8.59E-10	8.82E-10	8.60E-10
Power Dissipation (W)	1.46E-05	6.81E-11	1.46E-05	7.71E-11
Energy Dissipation (J)	5.68E-14	5.85E-20	1.29E-14	6.63E-20

4 CONCLUSION

The goals of this research are met by proposing a Gates Tied Mode dependent Dynamic D flip flop with enhanced average power and delay. Furthermore, when using GNRFETs instead of MOS, power dissipation is increased. Short channel effects are minimised in 16nm by using MOS including GNRFETs. GNRFET ribbon architectures offer improved low-power systems and thus a suitable replacement for standard MOS in shorter technology lengths. As compared to its MOS counterparts, the average power circuit is improved by 93.9 percent, the propagation delay is improved by 92.5 percent, and power dissipation is improved by 99.9 percent.

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